

Model Name: GA-B85N

Revision 1.11

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	ITE 8620 LPC IO
16	COM,KB_USB30
17	HWM,FAN CTRL,OV,-PROCHOT
18	DUAL BIOS
19	FP,FUSB,SPK,SATALED
20	Realtek ALC898
21	REAR AUDIO JACK
22	USB DAC POWER, mini PCI-E
23	INTEL LAN I217V
24	DISCRETE POWER
25	ATX,CLK GEN
26	RT8120_DDR POWER,M3 POWER
27	VCORE ISL95820_1

SHEET

TITLE

28	VCORE ISL95820_2
29	DVI-I
30	HDMI+USB2.0*2

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Cover Sheet

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Revision 1.11

Component value change history

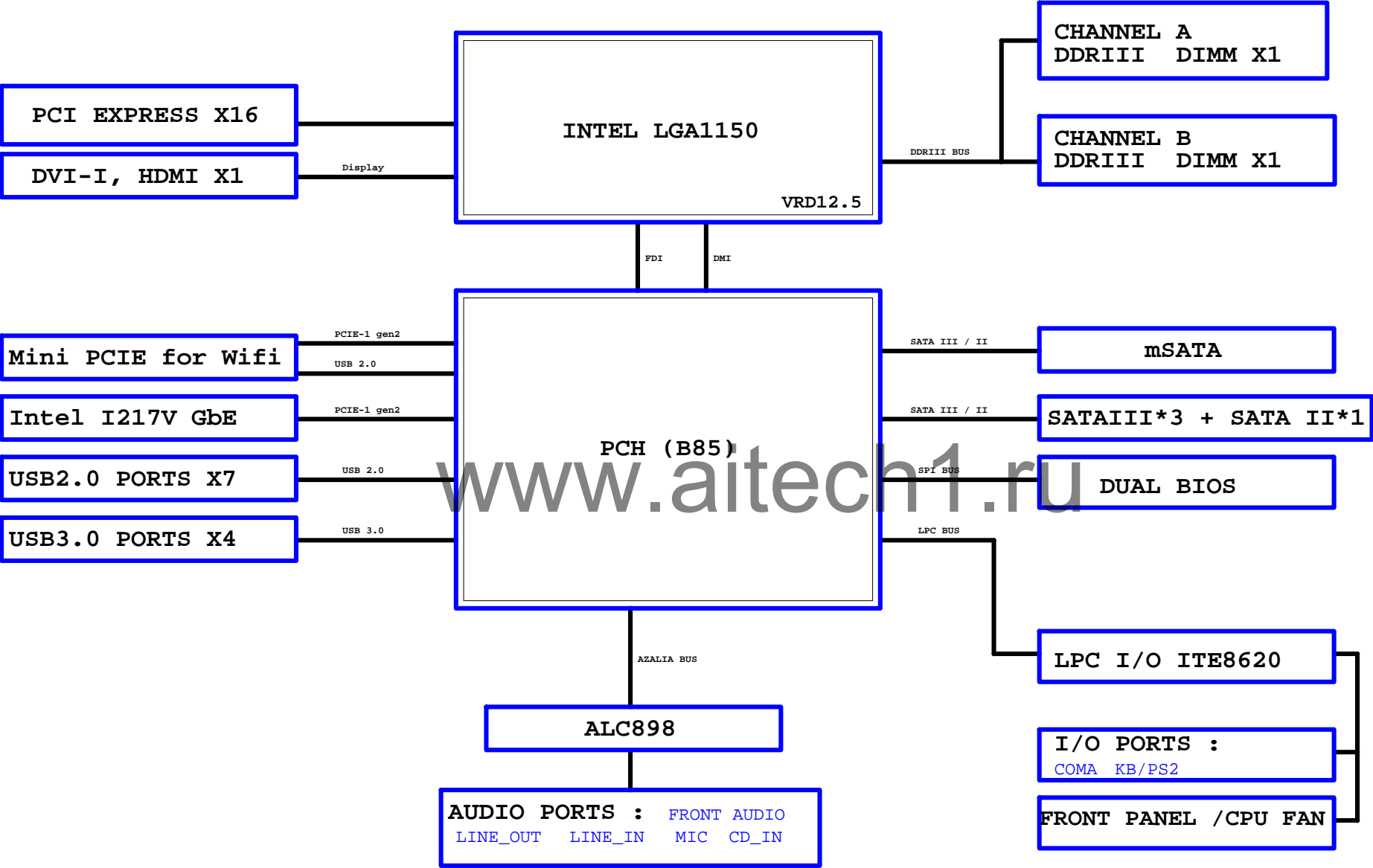
2013/07/02

[illegible]

Circuit or PCB layout change

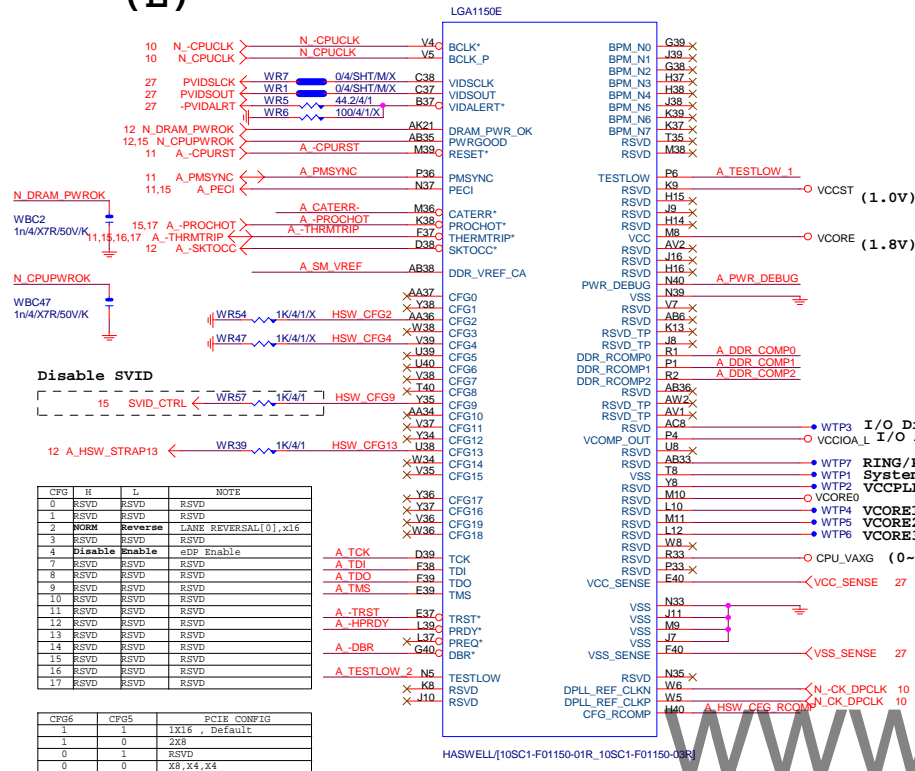
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BLOCK DIAGRAM



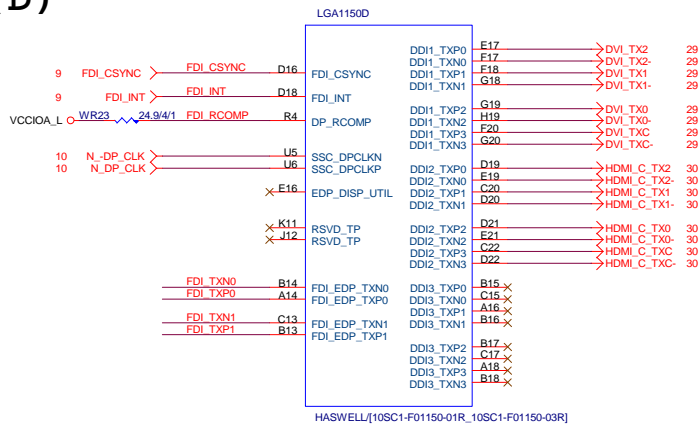
LGA1150

(E)



LGA1150

(D)



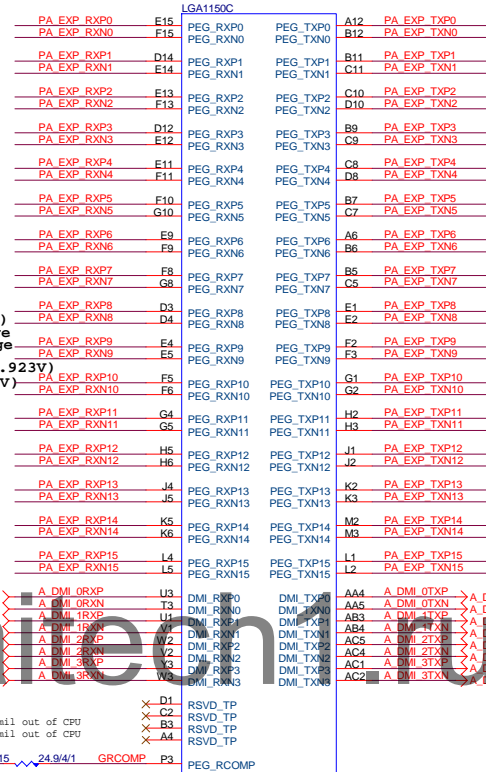
FDI:12/4/5/4/12(breakout min 6/4/4/4/6)
Impedance=85 +- 17.5%

FDI_TXP0_11 → FDI_TXP[0..1] 9
FDI_TXN0_11 → FDI_TXN[0..1] 9

LGA1155

(C)

PCIEX16:16/5/5/5/16(breakout min 10/4/4/4/10)
Impedance=80 +- 17.5%



DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

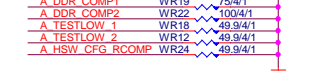
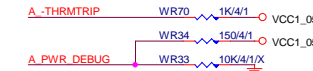
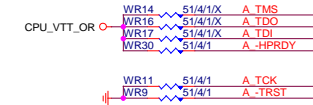
PA_EXP_TXP0_15 → PA_EXP_TXP[0..15] 14
PA_EXP_TXN0_15 → PA_EXP_TXN[0..15] 14
PA_EXP_RXP0_15 → PA_EXP_RXP[0..15] 14
PA_EXP_RXN0_15 → PA_EXP_RXN[0..15] 14

-CPURST

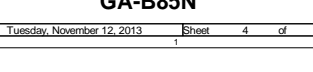
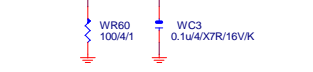
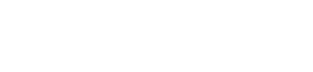
CPU SVID

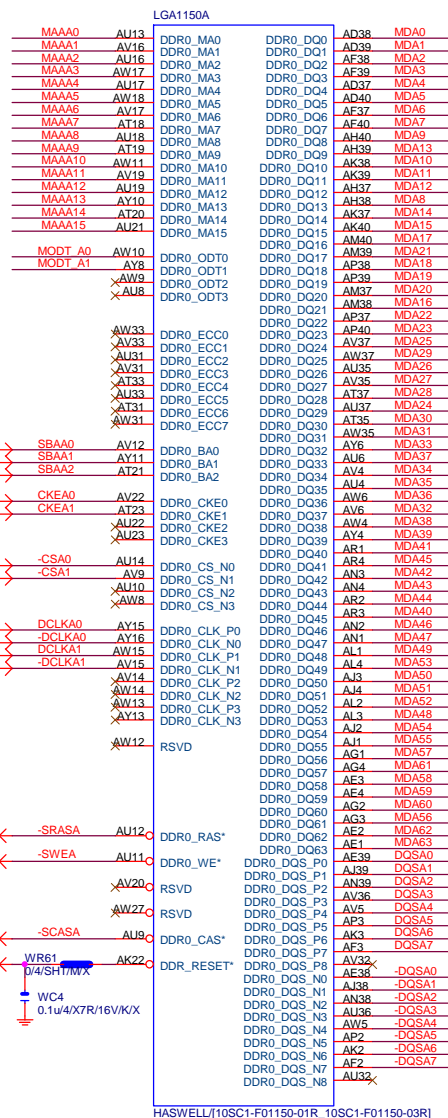


CPU PU/PD

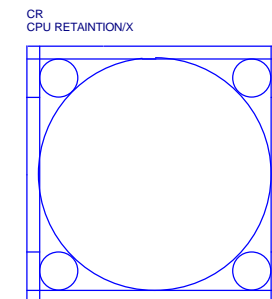
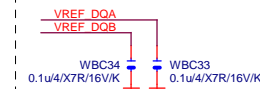


SM REF





Place in CPU bottom side



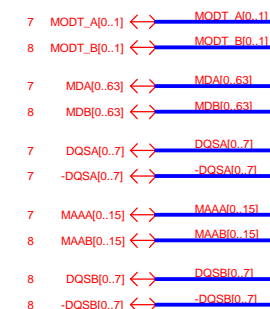
LGA1150



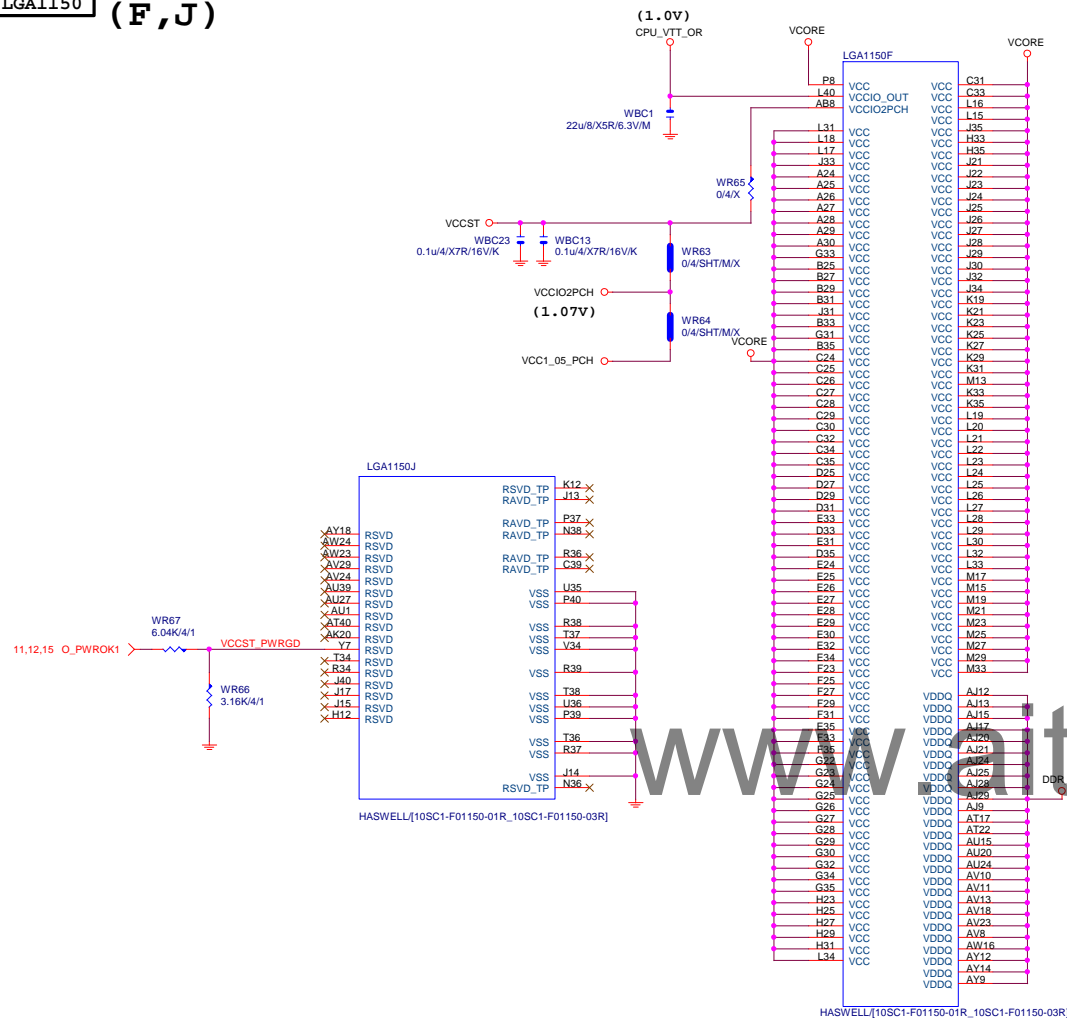
COVER+BLACK NI

ILM_BP/1156/BKNI/12KRC-0F0001-61R_12KRC-0F0001-62R

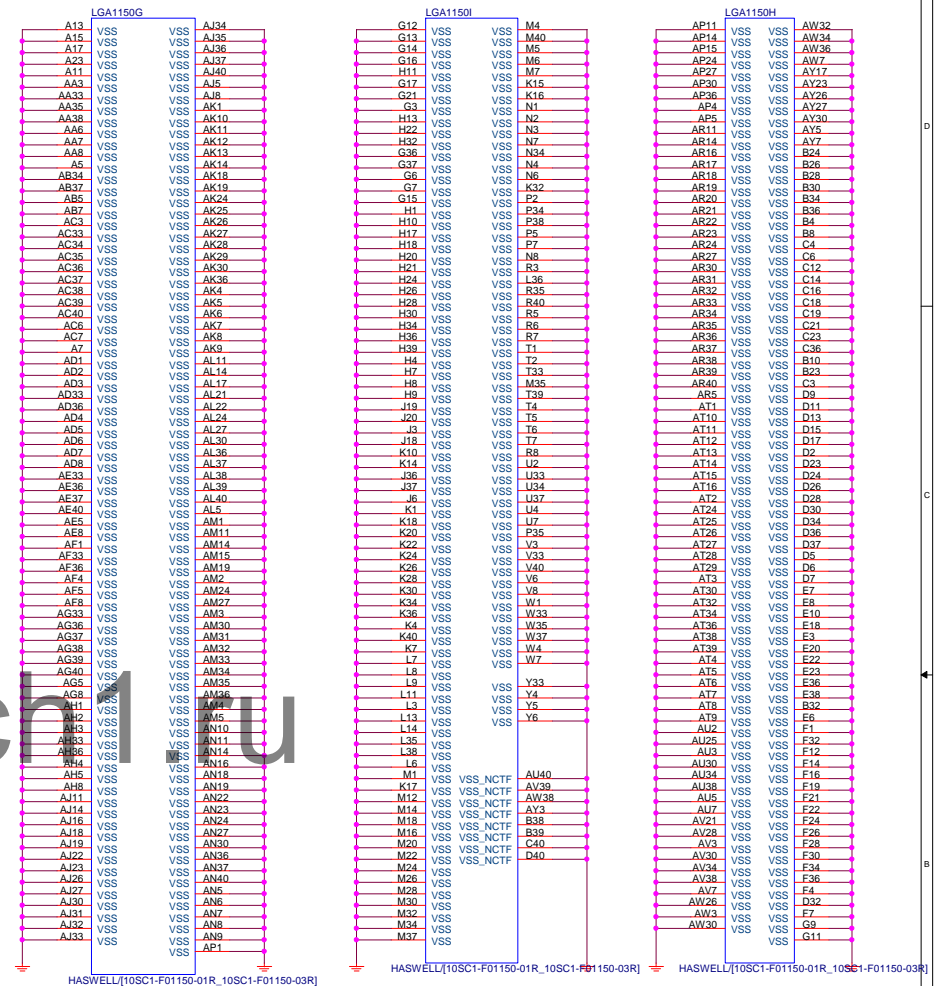
DDR BUS



LGA1150 (F, J)

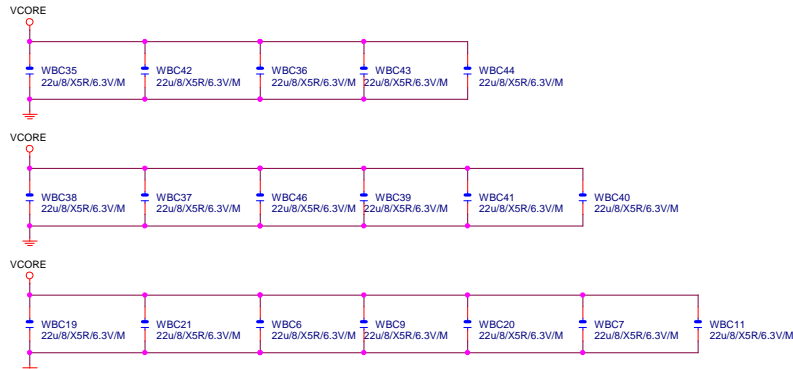


LGA1155 (G,H,I)



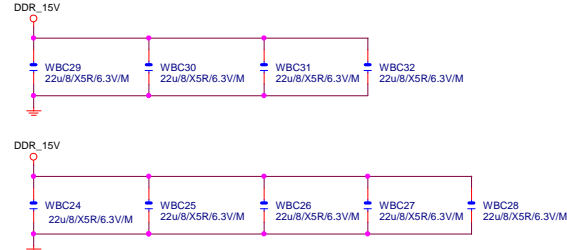
VCore CAP

(x18)



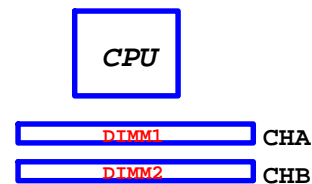
DDR CAP

(x9)



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Title			
CPU LGA1150-C			
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DMI:12/4/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

VCC1_5_PCH

NR50 7.5K/4/1 DMI_COMP

NR40 7.5K/4/1 PCIE_COMP

CK_SRCCLK_PCH

CK_SRCCLK_PCH

IB
I217

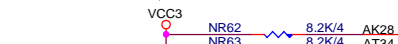
Figure 1. A schematic diagram of the experimental setup. The subject is seated in a chair, viewing a screen displaying a target (a red dot) and a starting point (a black dot). The subject's hand is positioned at the starting point, and the target is located at a distance of 10 cm from the starting point. The subject is instructed to move the hand to the target. The distance between the starting point and the target is labeled as 10 cm. The subject's hand is shown in a starting position, and the target is shown as a red dot on the screen. The distance between the starting point and the target is labeled as 10 cm.

```
PCIEX1:16/5/5/5/16 (breakout_min_8/4/4/4/8)
```

PCHB	B85: Port 6/7 N/A
	H81: Port 6/7/12/13 N/A



4/4/4/8)



OK SRCCLK F

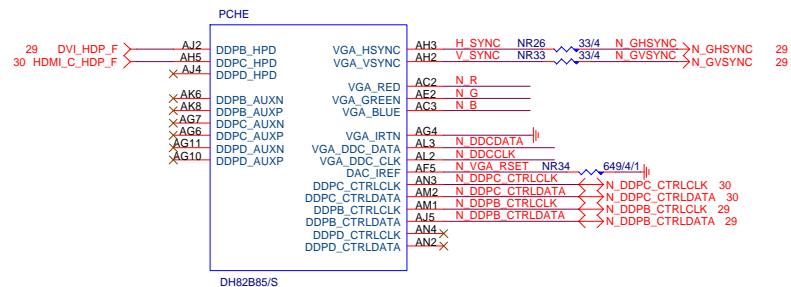


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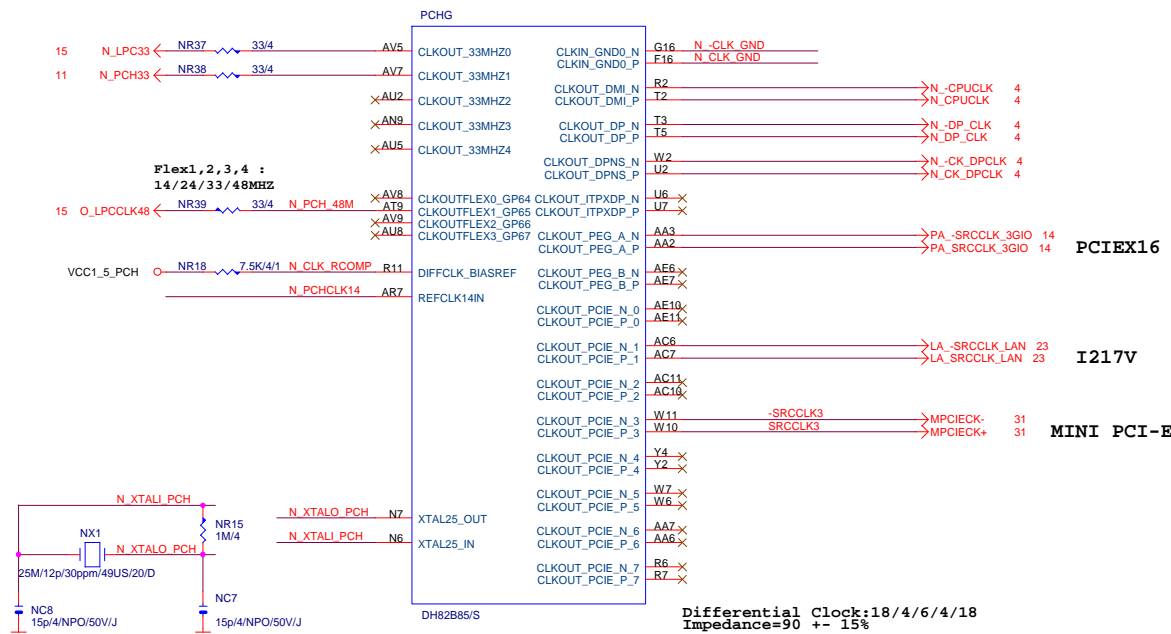
PCH.FDI.DMI.USB.PCI.E.NVRAM

Title			
PCH FDI,DMI,USB ,PCIE,NVRAM			
Size	Document Number		Rev
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PCH (E)



PCH (G)



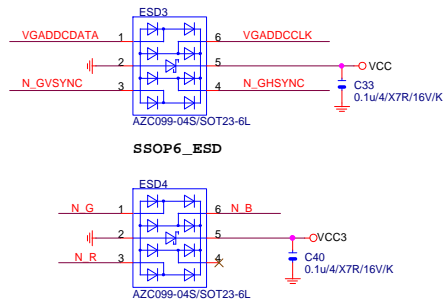
PCH CLK PD



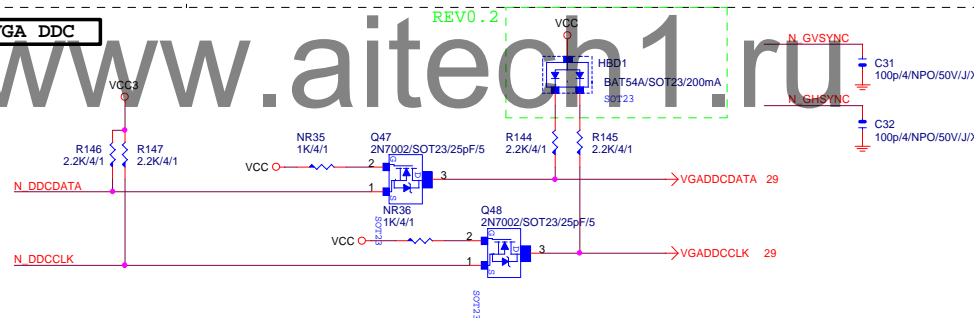
Mount for integrated clock Generation
Mode



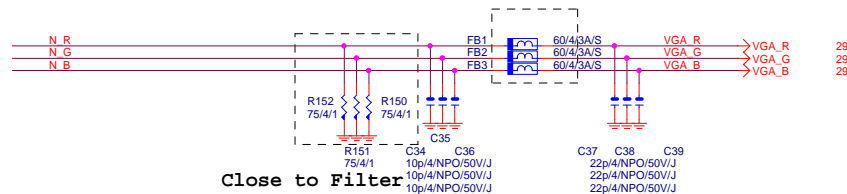
VGA ESD



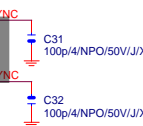
VGA DDC



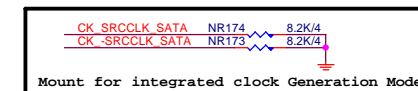
VGA DDC



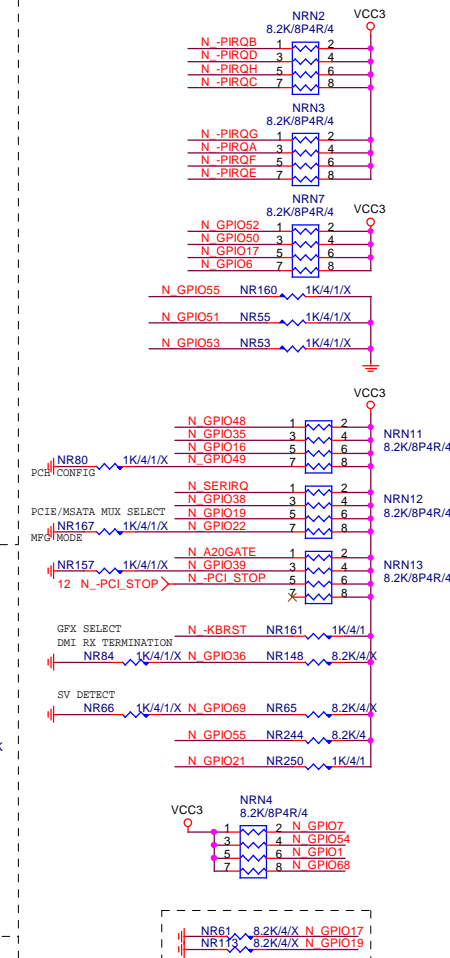
VGA CONNECTOR



SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%



PCH	PU/PD
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SATA3_0
 SATA2/7/WH/OP/VA/D/1/B/PA66
BLACK CONNECTOR

SATA3_1
 SATA2/7/WH/OP/VA/D/1/B/PA66
BLACK CONNECTOR

SATA3_2
 SATA2/7/WH/OP/VA/D/1/B/PA66
BLACK CONNECTOR

H81 Port 2/3 N/A

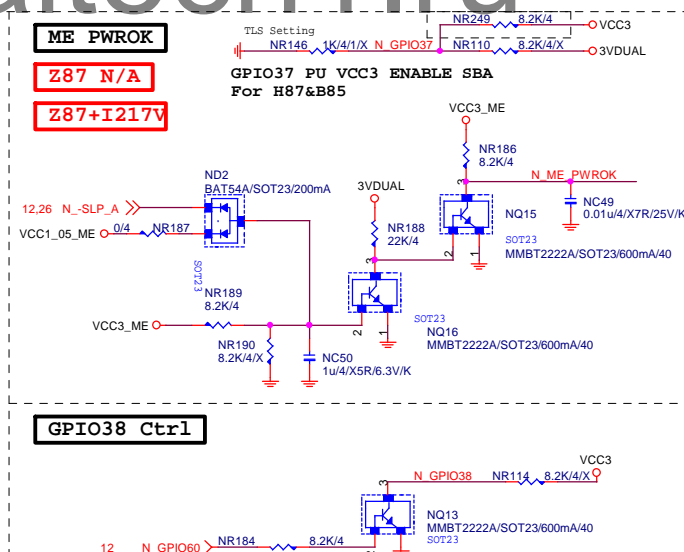
**** Z87/H87 Port 4&5 SATA3.0**
**** B85 Port 4&5 SATA2.0**

N/A

Z87 N/A

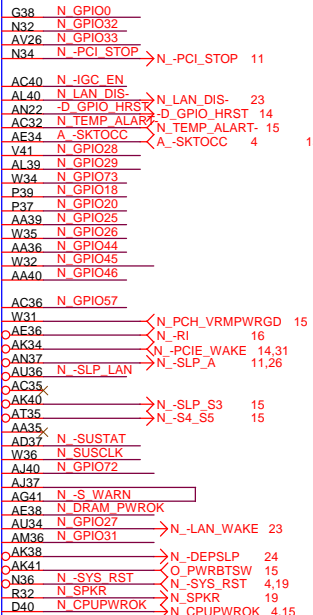
787+T3175

Z87+I217V

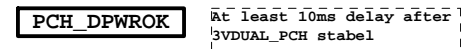


GPIO38 Ctrl

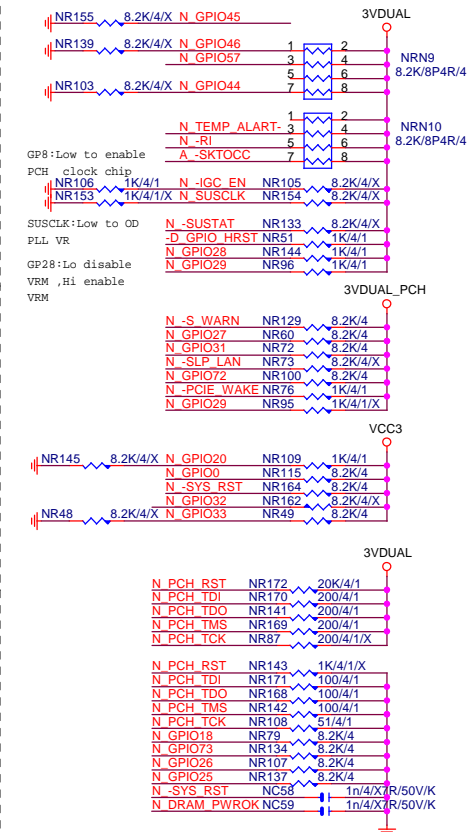
(D)



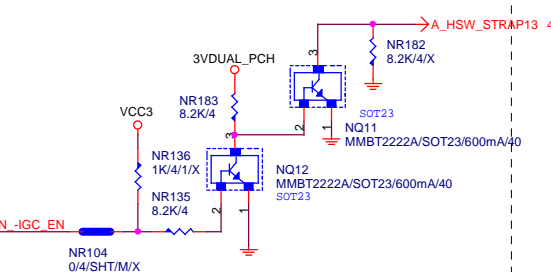
ACZ SDOUT



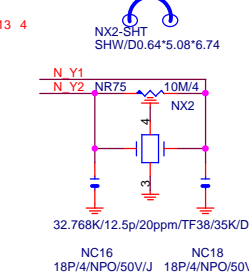
PCH	PU/PD
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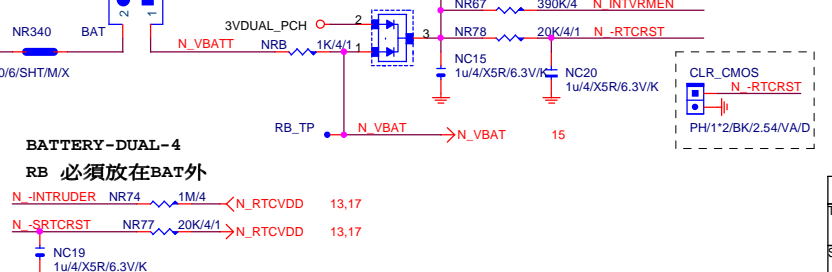
HSW_STRAP13



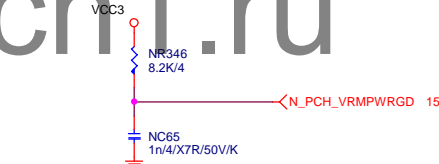
32.768KHZ



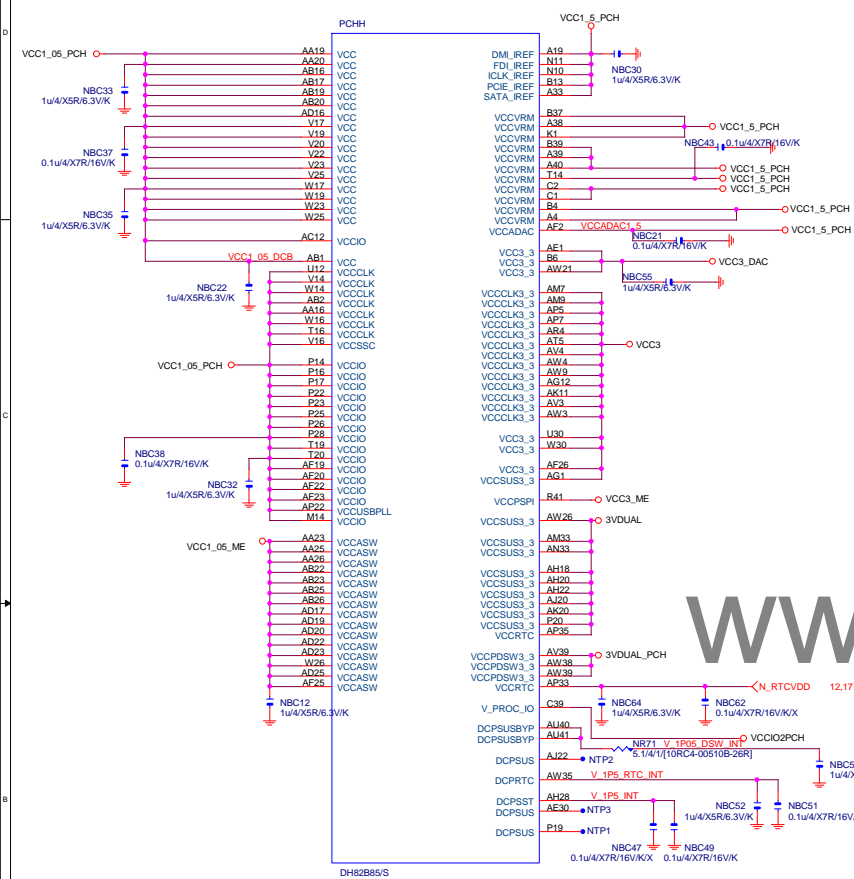
CLR_CMOS



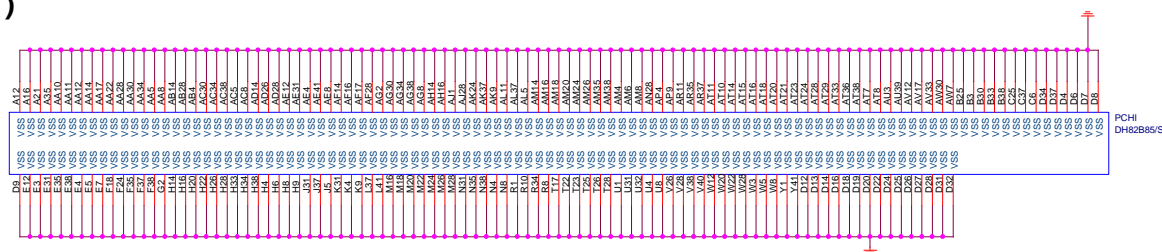
CPU VRDY



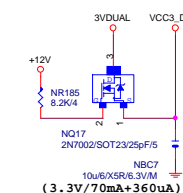
PCH (H)



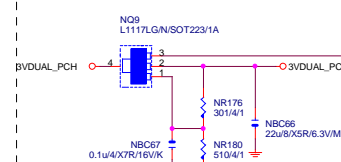
PCH (I)



VCC3_DAC

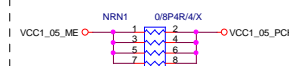
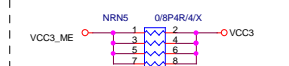


3VDUAL_PCH



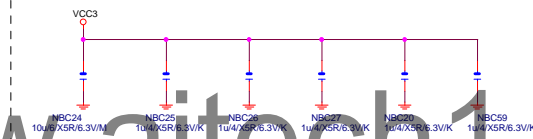
SHT PWR

M3 POWER

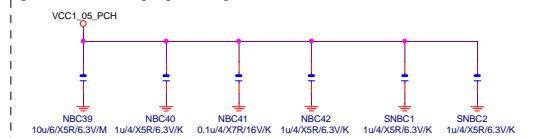


CAP

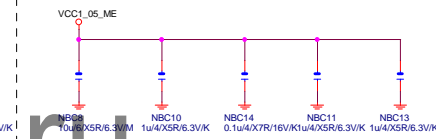
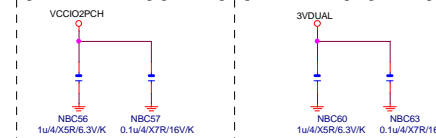
(3.3V) (X6)



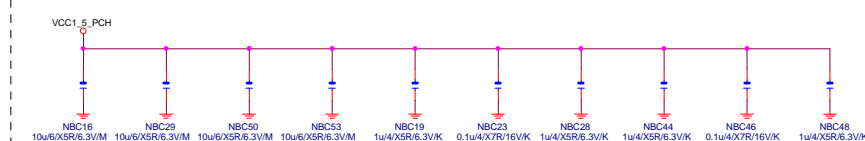
(1.05V)(x6)



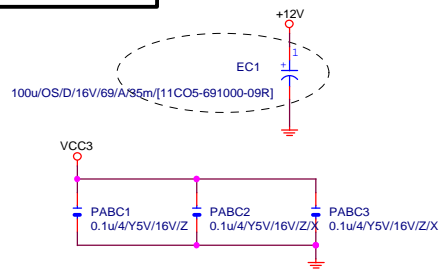
(1.05V) (x5)


$$(1.05V)(x2) \quad (3.3V)(x2)$$


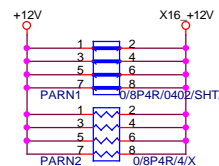
(1.05V) (x10)



PCIEX16 CAP



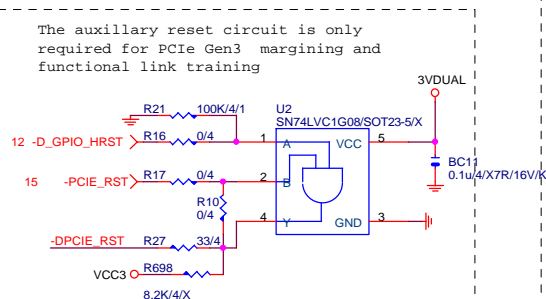
PCIEX16 PROTECT SHT



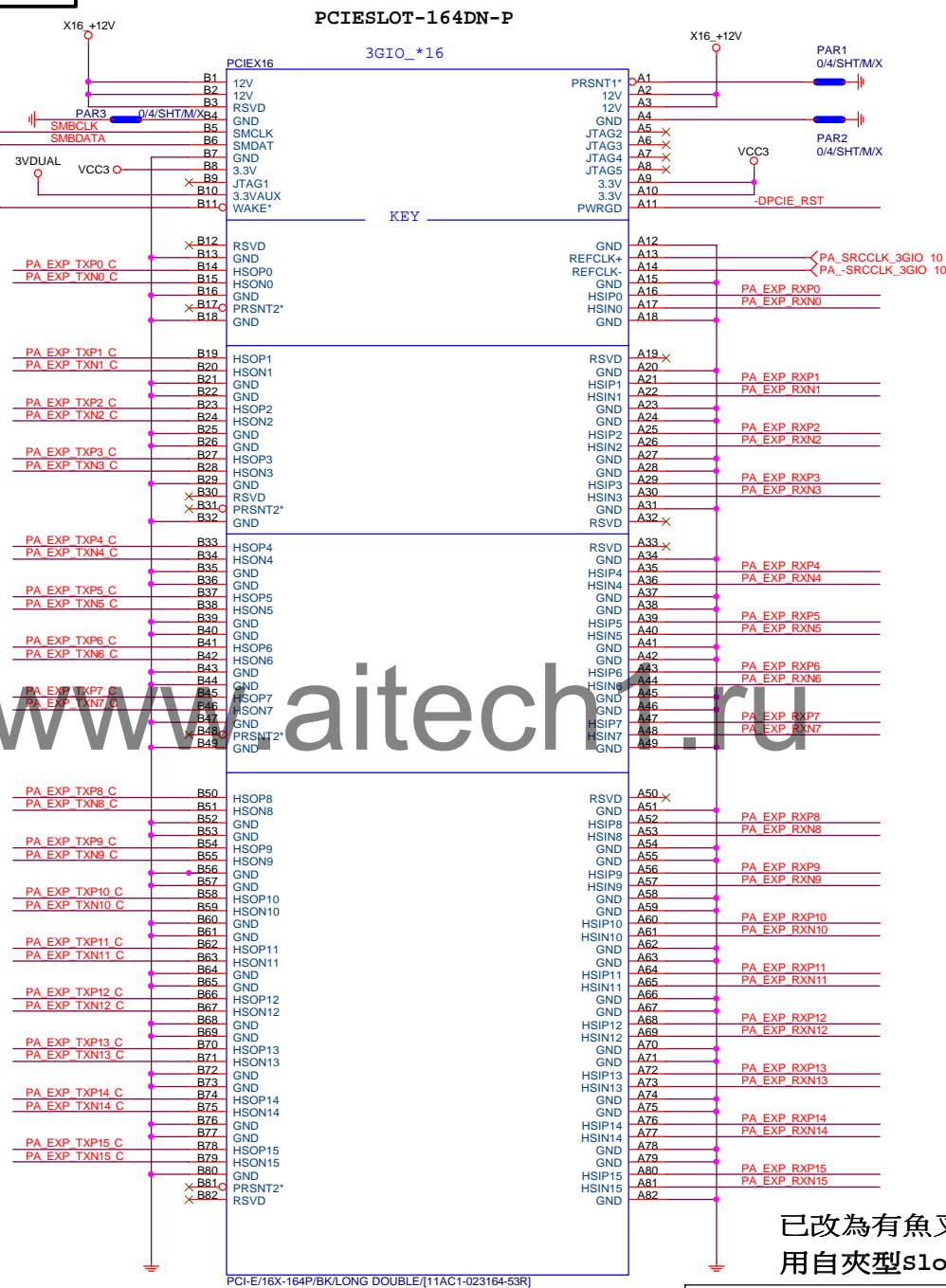
PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
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PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

```
PA_EXP_RXP[0..15] >> PA_EXP_RXP[0..15] 4
PA_EXP_RXN[0..15] >> PA_EXP_RXN[0..15]
PA_EXP_TXP[0..15] >> PA_EXP_TXP[0..15] 4
PA_EXP_TXN[0..15] >> PA_EXP_TXN[0..15] 4
```



PCIEX16 SLOT



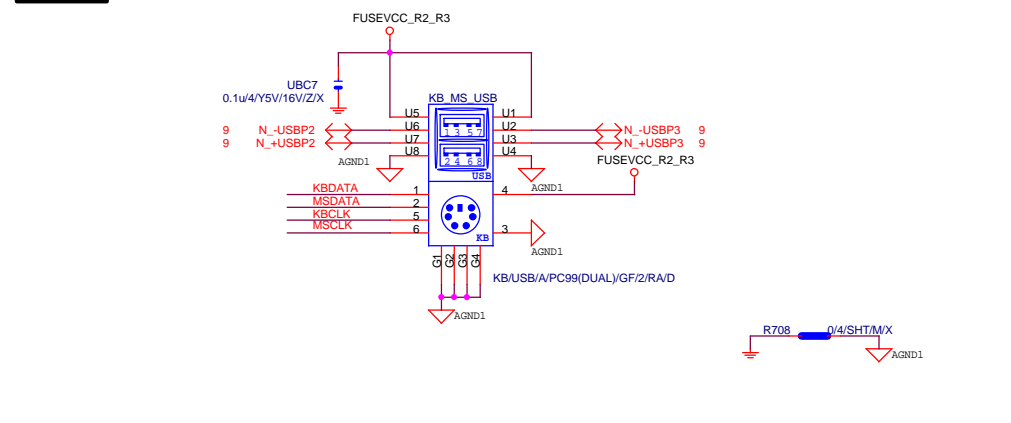
已改為有魚叉腳的slot
用自夾型slot

BLACK CONNECTOR

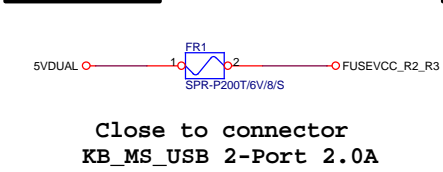
Gigabyte Technology

Title			
PCI EXPRESS * 16			
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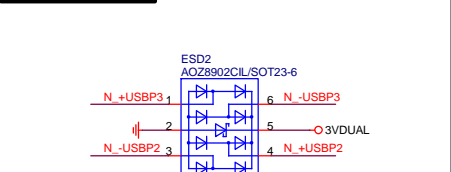
KB/MS



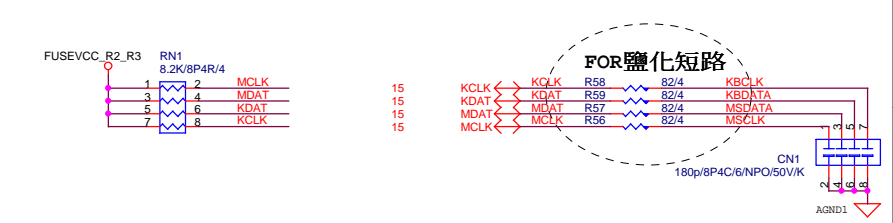
USB2.0 PWR



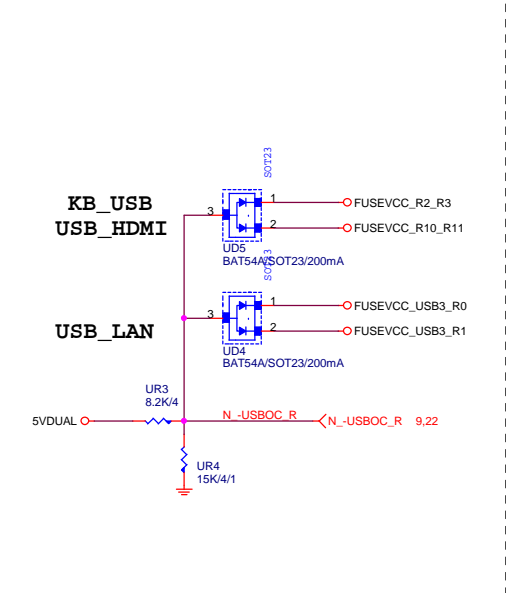
USB2.0 ESD



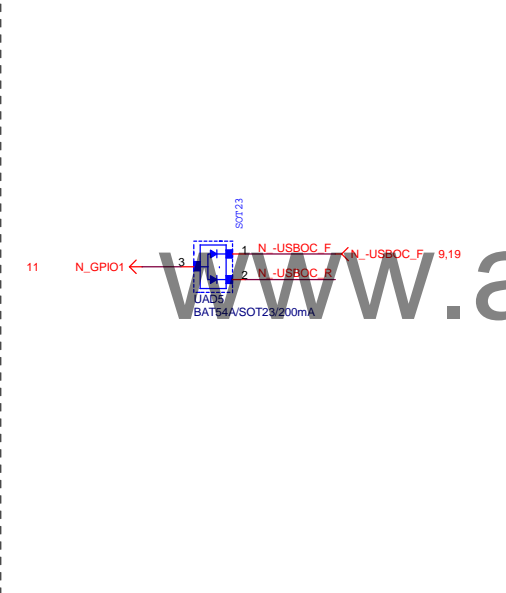
KB_MS



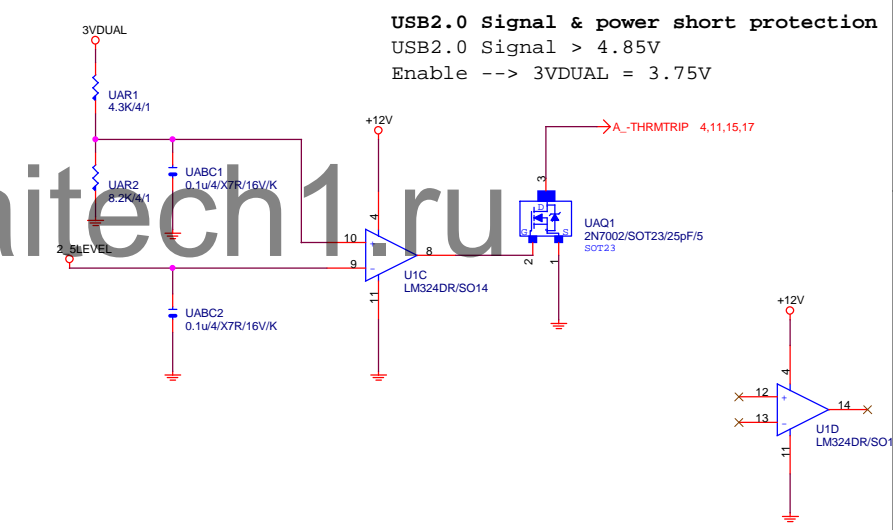
-USBOC_R



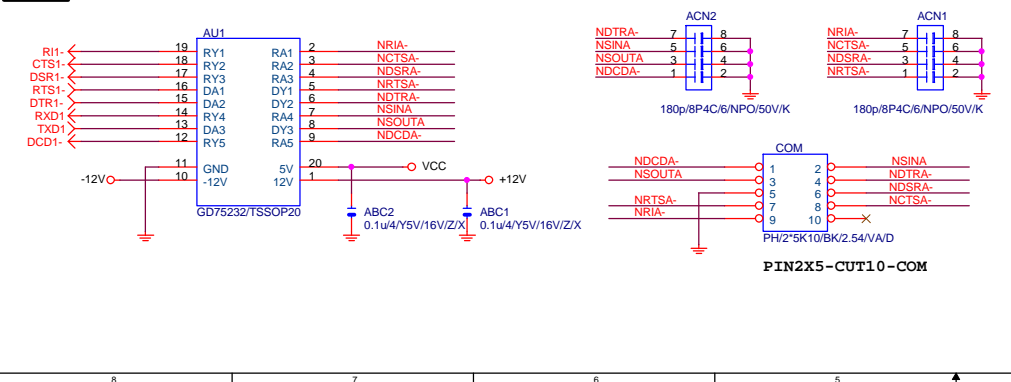
USB POWER PROTECT



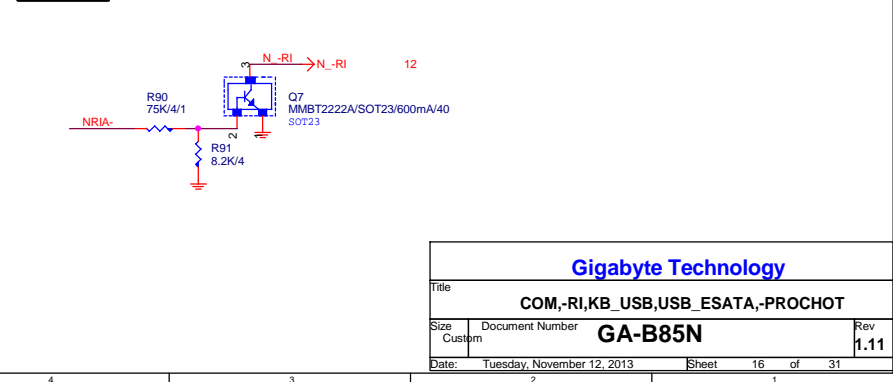
USB2.0 Short Power Protection



COM



COM RI



15 VREF ←

15 SYS_TEMP ←

15 PCH_TEMP ←

15 TEMP3 ←

C8 1u4/X5R/6.3V/K

C10 1u4/X5R/6.3V/K

R36 10K/4/1

R40 8.2K/4

R42 8.2K/4

RS_SYS 10K/1/4/S

Close S10

CASE OPEN

12,13 N_RTCVDD

R88 1M4

R709 0/4/SHT/X

N_INTRUDER 12

-CASEOPEN 15

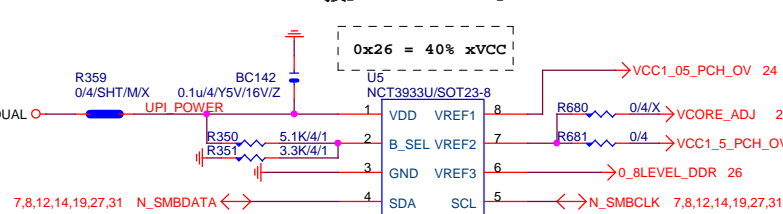
PWR GLITCH

C25 1u4/X5R/6.3V/K

CI PH'12/BK/2.54/VA/D

[illegible]

接pwm feedback pin



CPU SMART FAN

15 FANPWM1

100 μ S/D/16V/69/A/35m/[11CO5-691000-09R]

EC16

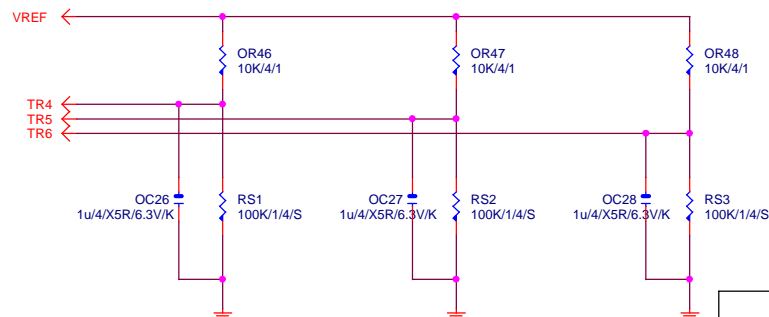
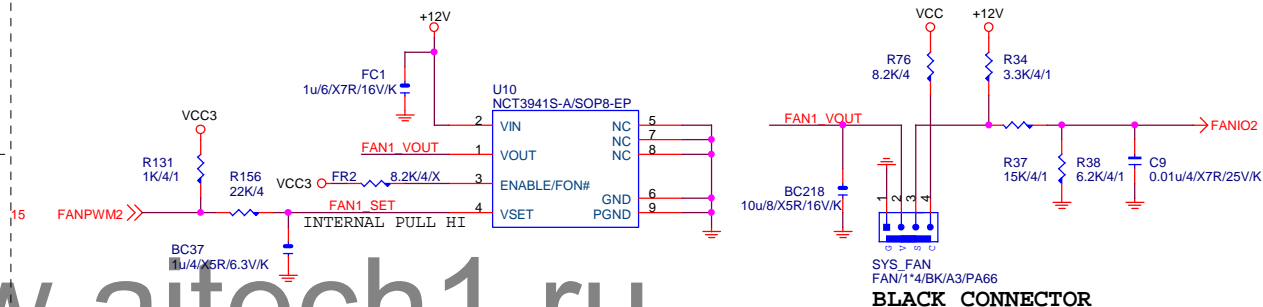
FOR HOT-PLUG ISSUE

C20
0.1 μ F/4/X7R/16V/K

CPU_FAN
FAN/1*4/WH/A3/PA66

BLACK CONNECTOR

Linear SYS_FAN



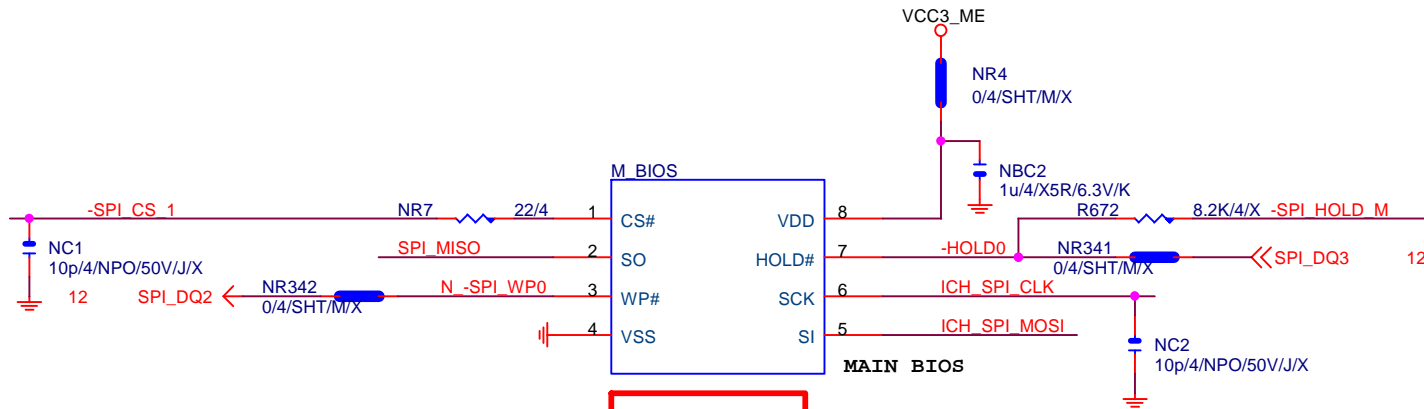
RS1、RS2、RS3 CLOSE CPU
VR MOSFET

Gigabyte Technology

HWM,FAN CTRL,OV

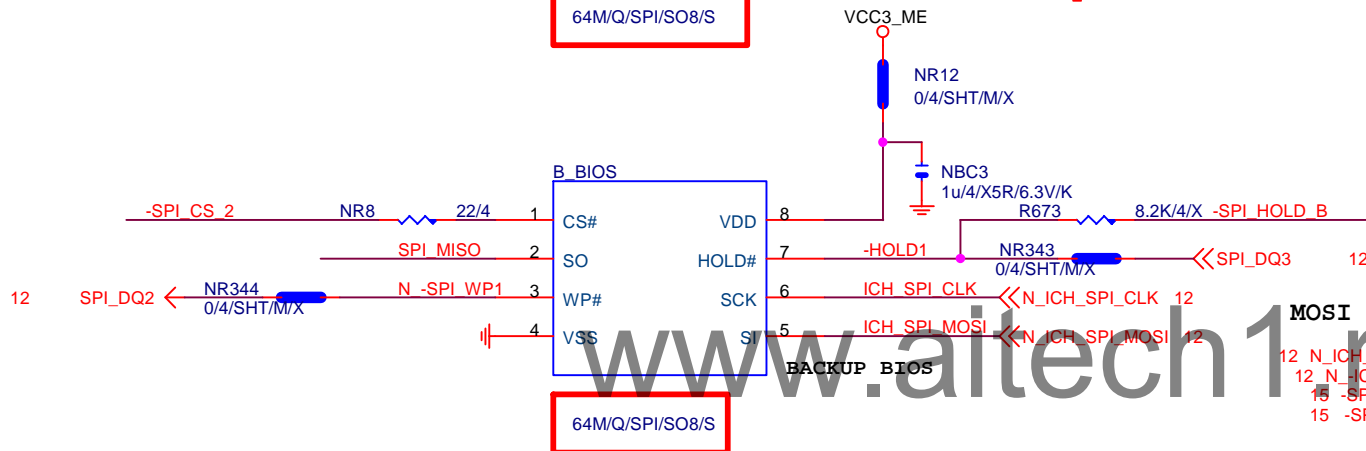
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1.11

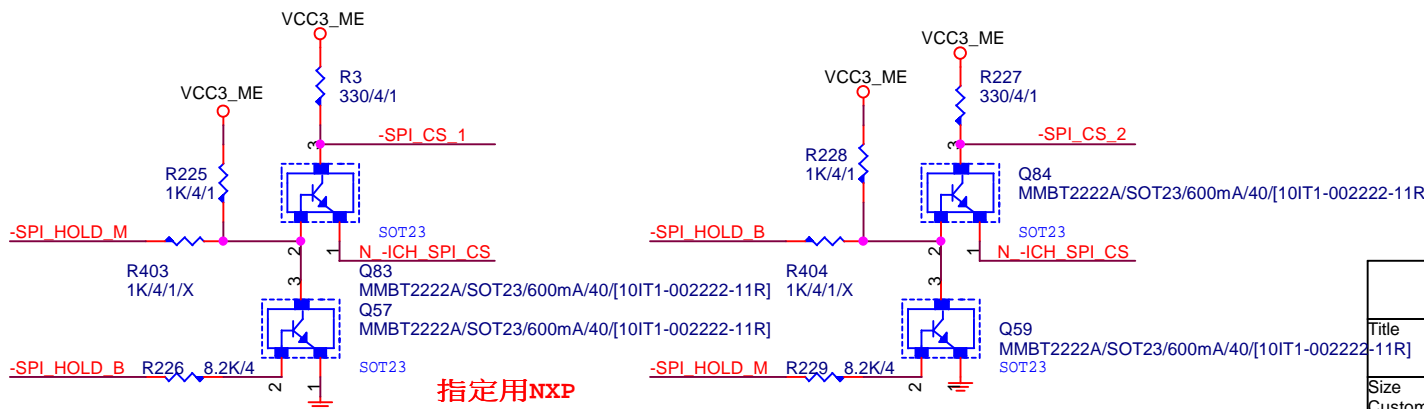
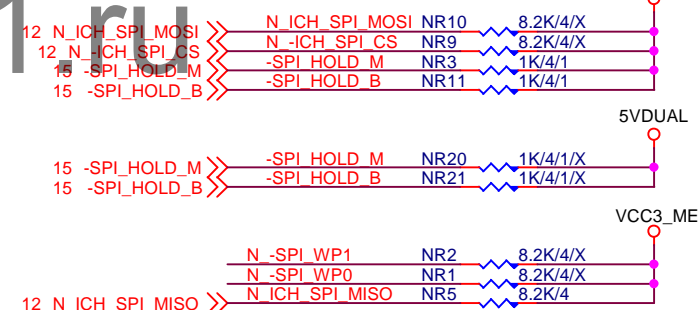


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

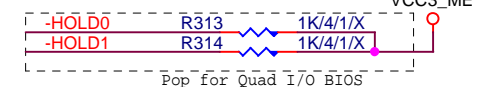
1 means floating
0 means PD 1K



MOSI For DMI RX Termination Voltage



CHECK

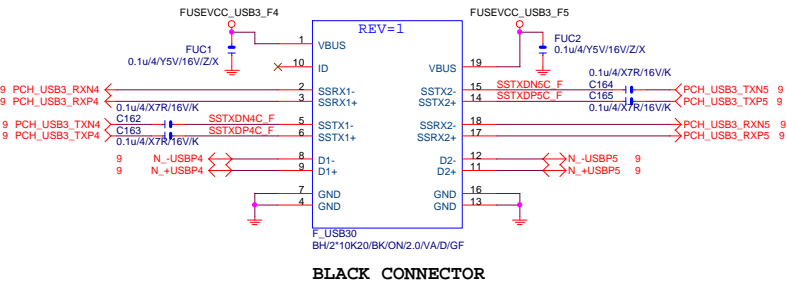


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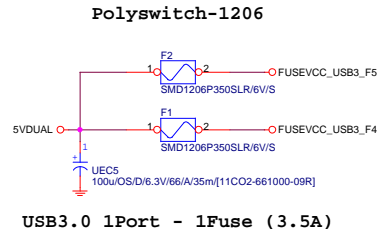
DUAL BIOS

Title	GA-B85N	Rev	1.11
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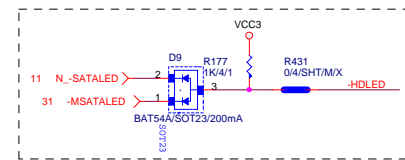
F_USB30



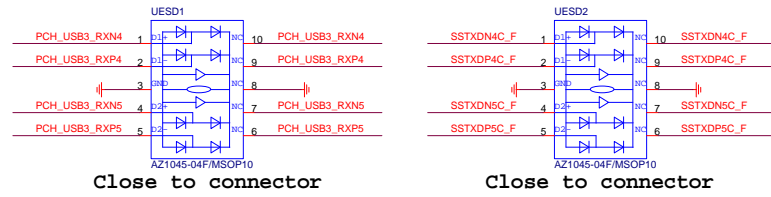
F_USB30 PWR



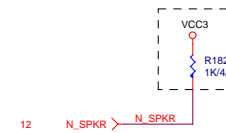
SATA_LED



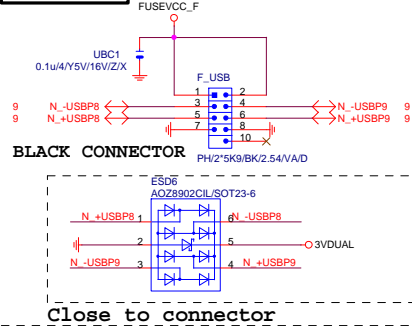
F_USB30 ESD PROTECT



SPKR



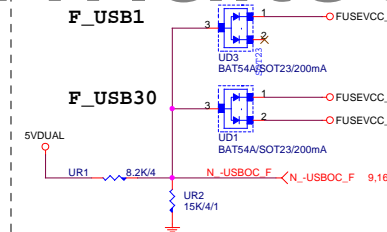
FRONT USB1



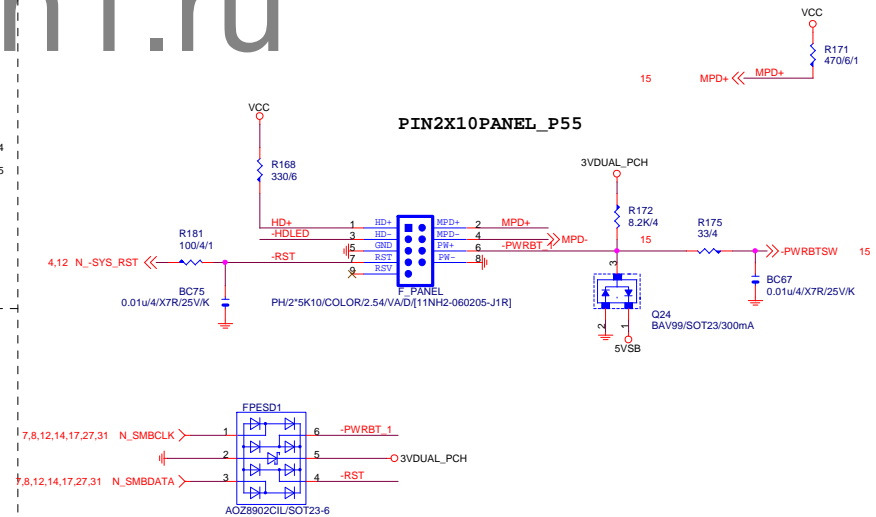
FUSEVCC_F

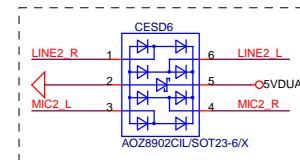


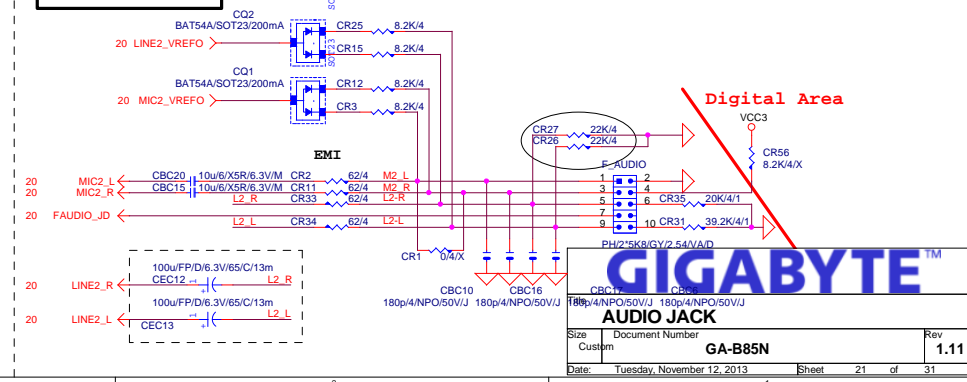
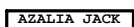
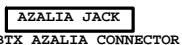
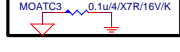
-USBOC_F



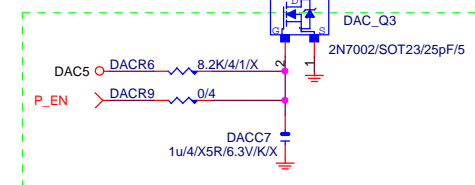
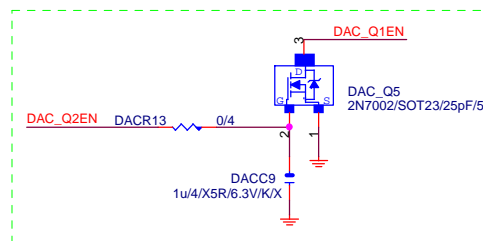
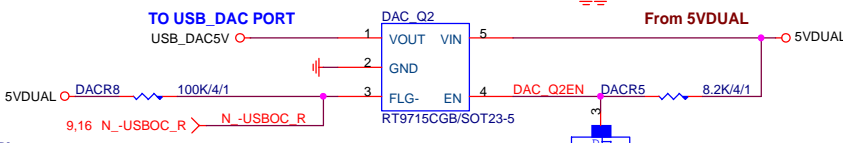
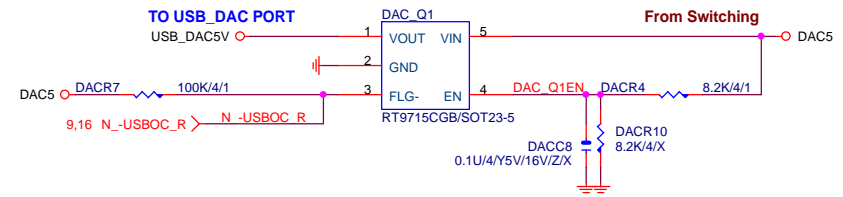
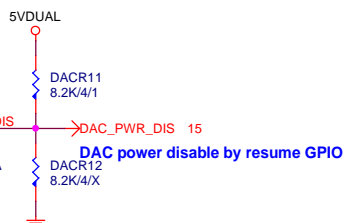
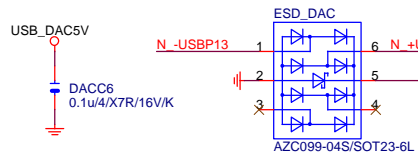
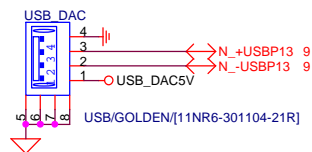
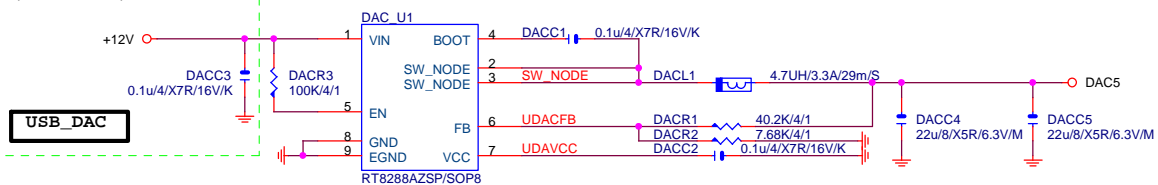
INTEL FRONT PANEL



[illegible]

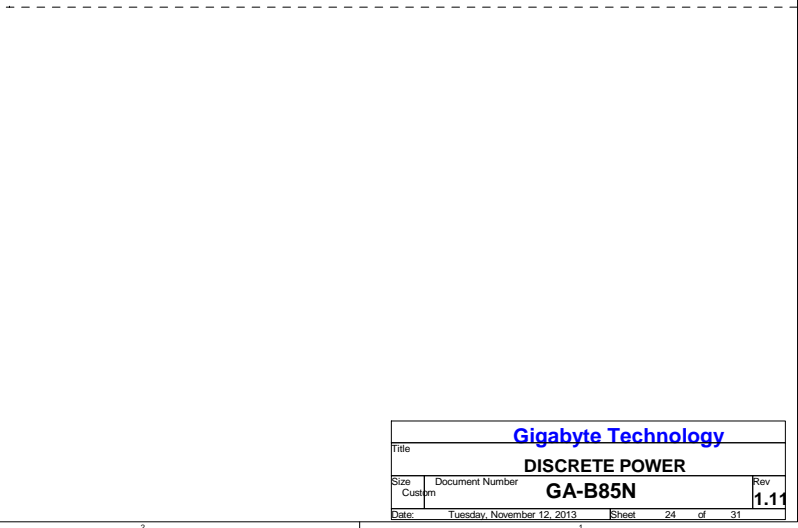
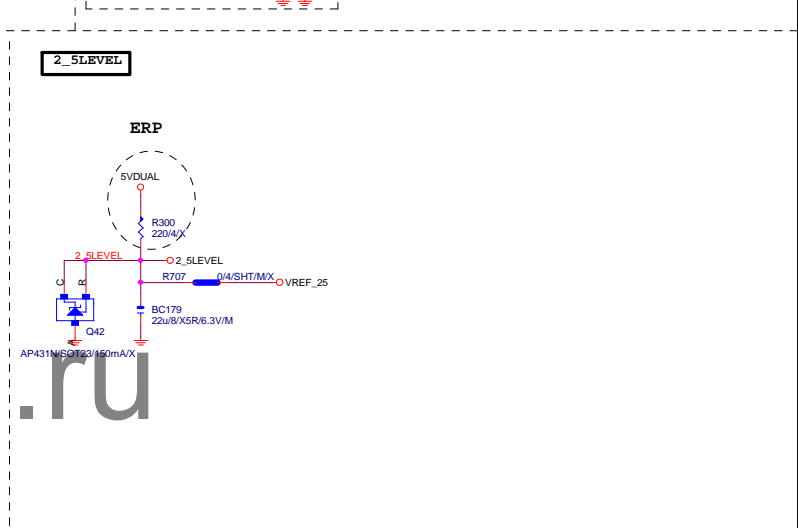
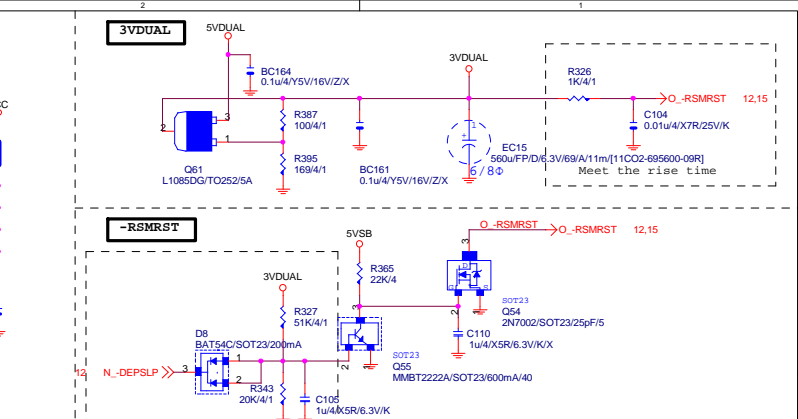


Remove DACD1 & DACR14
(For DFM)

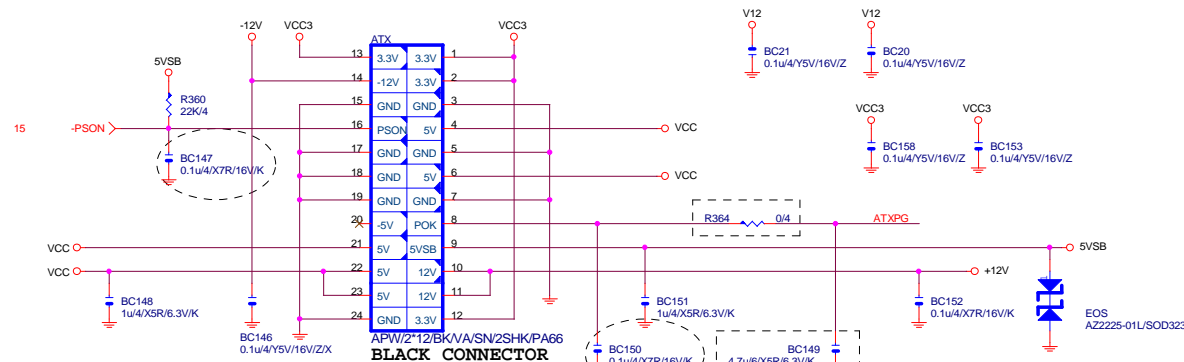


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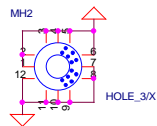
Gigabyte Technology			
Title			
USB DAC POWER			
Size	Document Number	Rev	
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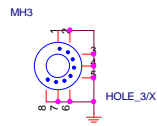
ATXX24 POWER CONNECTOR



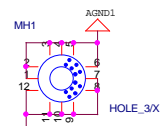
MB LOCATION



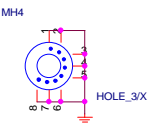
HOLE_4-RH-5MM-1



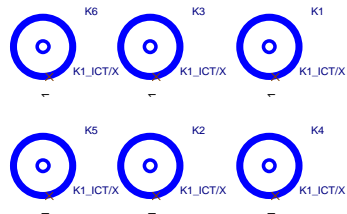
HOLE_4-RH-5MM-5PIN-1



HOLE_4-RH-5MM-1

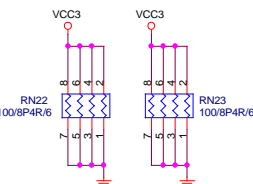


HOLE_4-RH-5MM-5PIN-1



To prevent the 5VSB under loading when boot

FIX PWR MINMUN LOAD



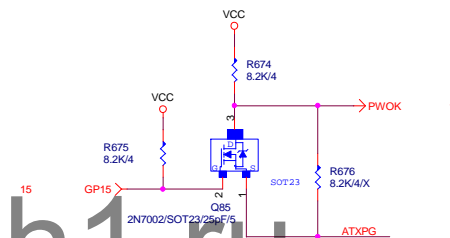
ATXX4 POWER CONNECTOR



ATX_4-6
BLACK CONNECTOR

PWOK PATCH

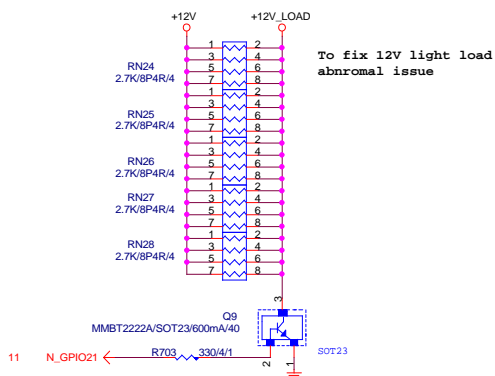
【技術通報R&D技術通報154】



CLK GEN

N/A

【技術通報R&D技術通報153】



To fix 12V light load abnormal issue

Gigabyte Technology

ATX CONNECTOR

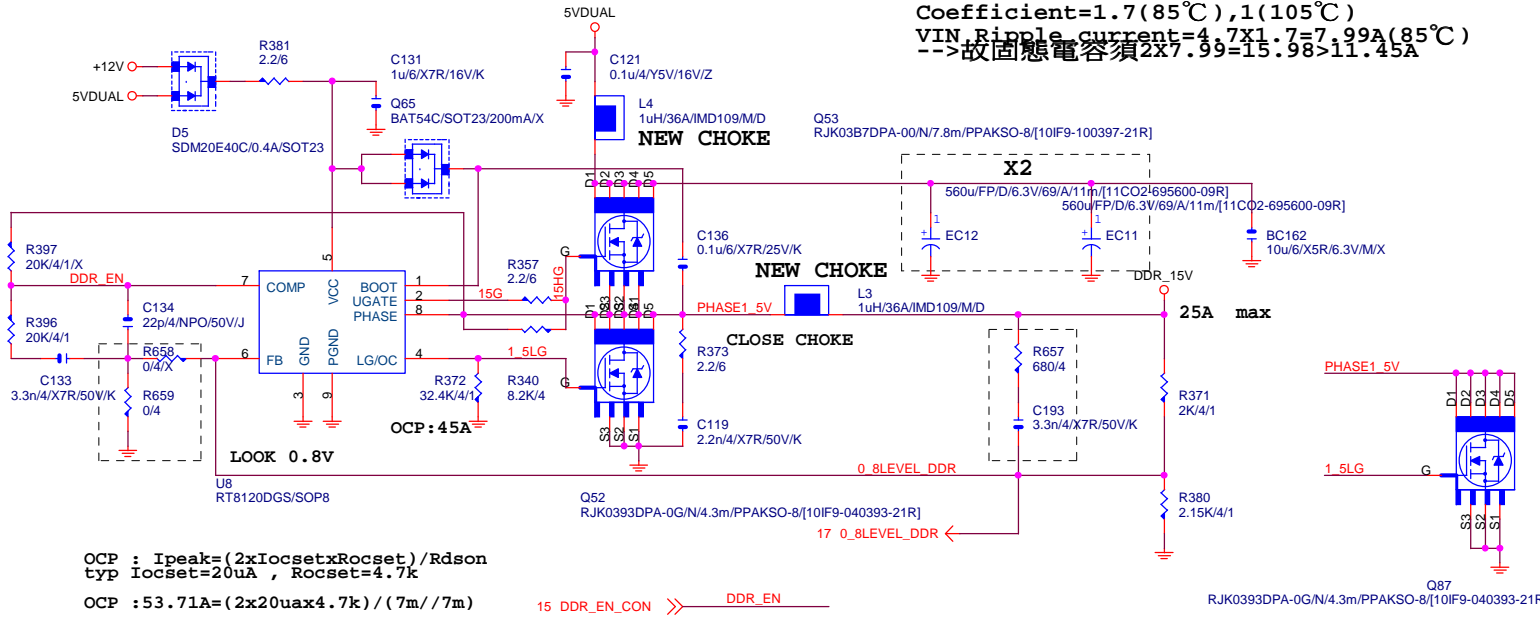
GA-B85N

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DDR15V

VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
 IRMS=11.45A
 560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
 Coefficient=1.7(85°C), 1(105°C)
 VIN_Ripple current=4.7x1.7=7.99A(85°C)
 --->故固態電容須 $2 \times 7.99 = 15.98 > 11.45A$

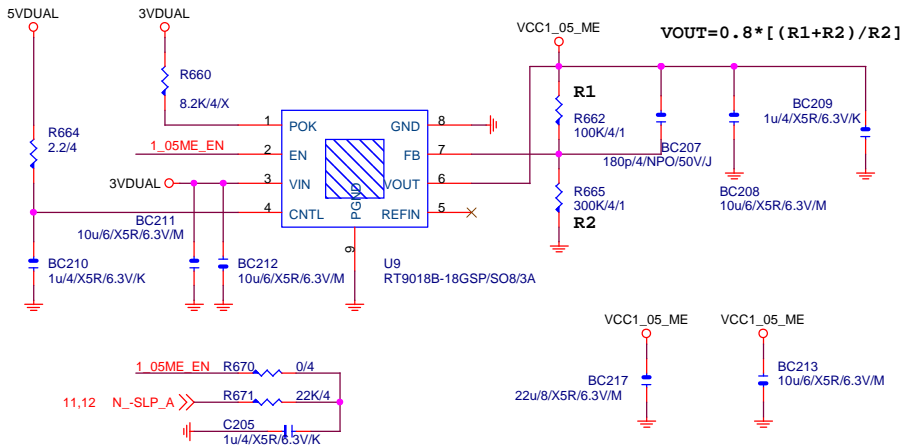


VCC1_05_ME

Z87 N/A

Z87+I217V

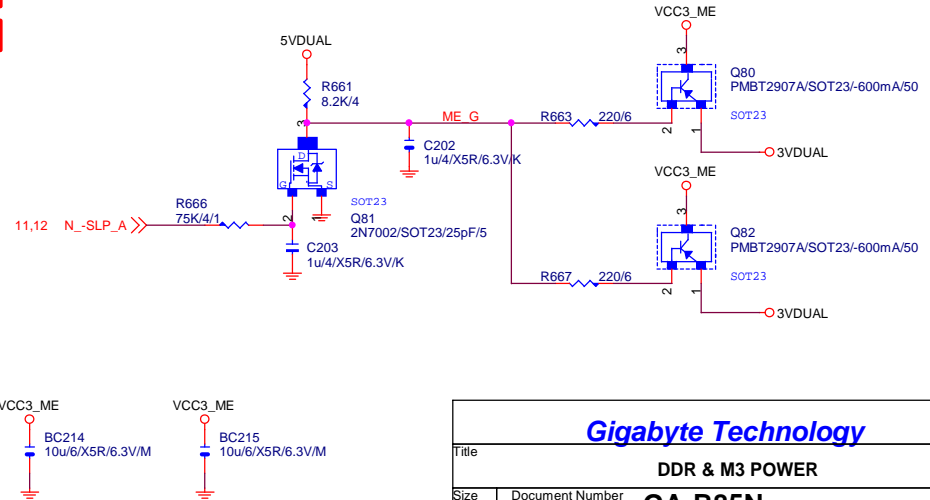
【技術通報R&D技術通報156】
 (RICHTEK), (NUVOTON), (EMC)做共用
 PIN7分壓阻值須做修改為100K以上電阻值



VCC3_ME

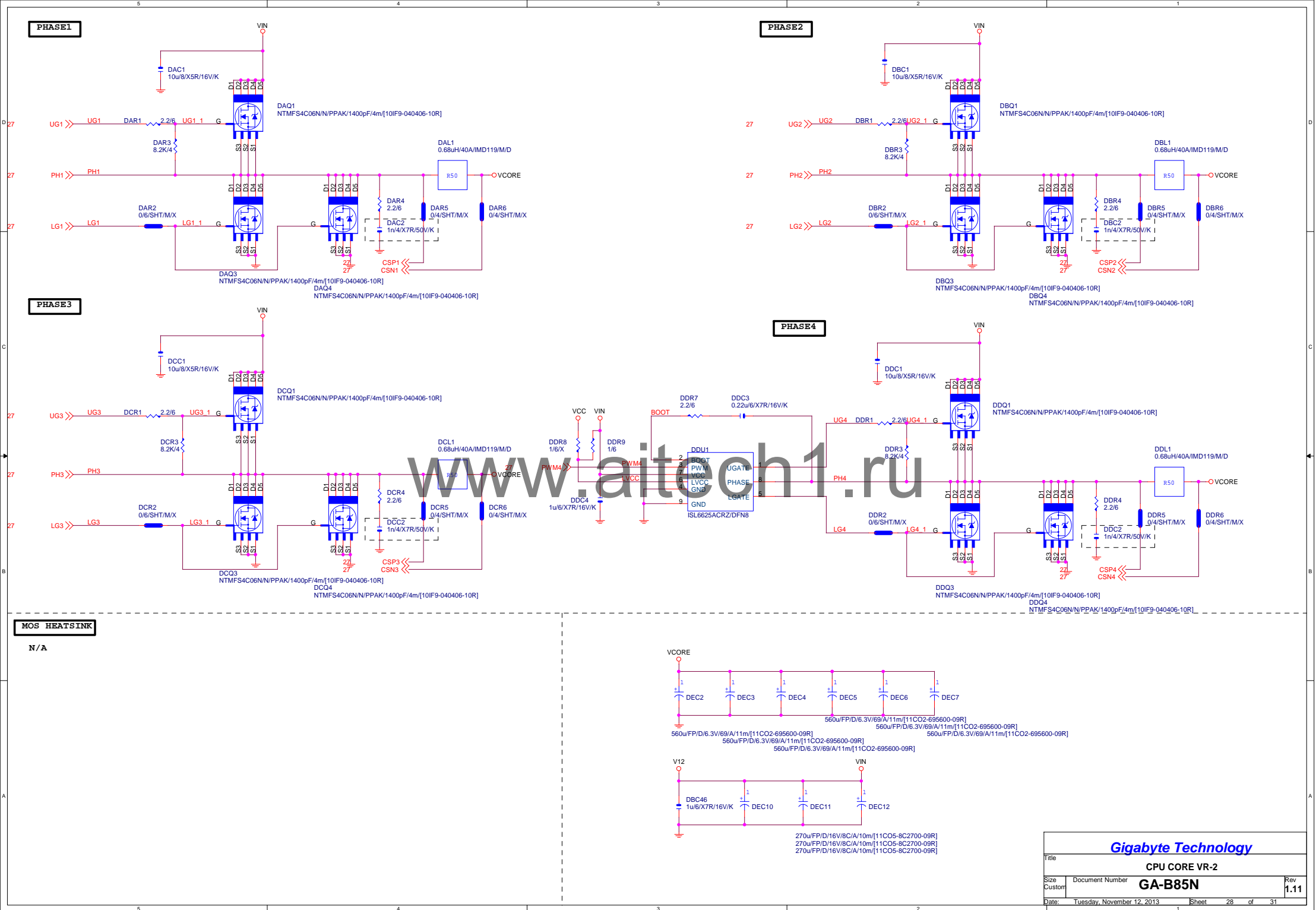
Z87 N/A

Z87+I217V

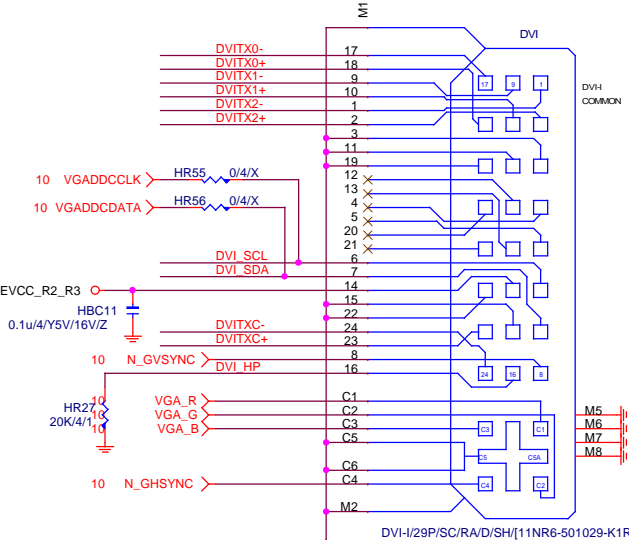
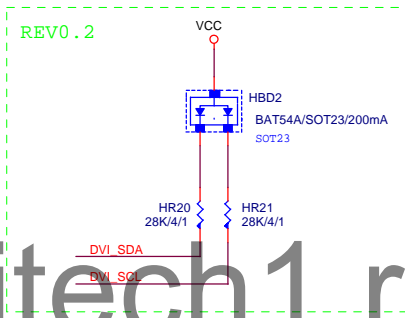
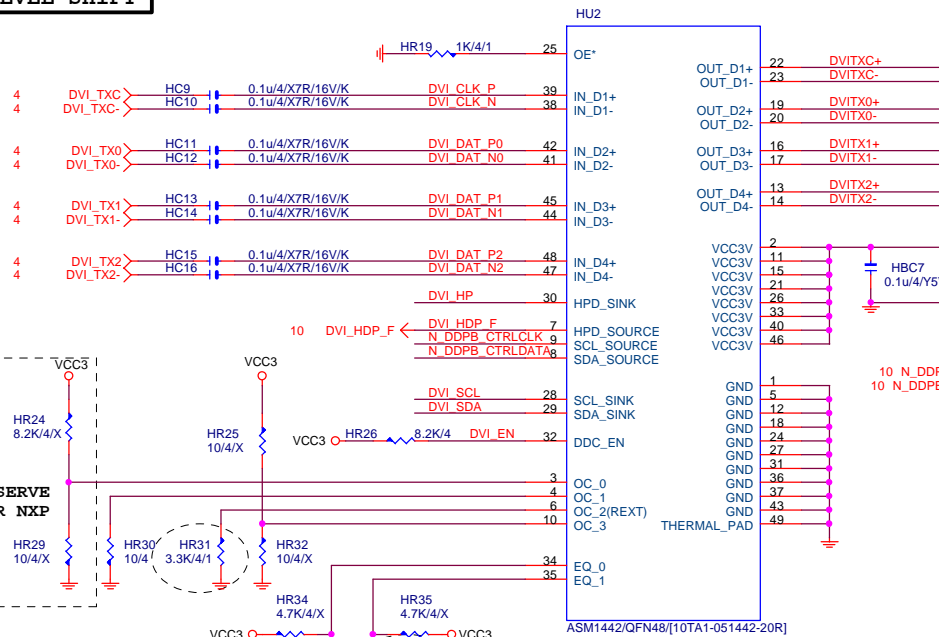


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Title		
DDR & M3 POWER		
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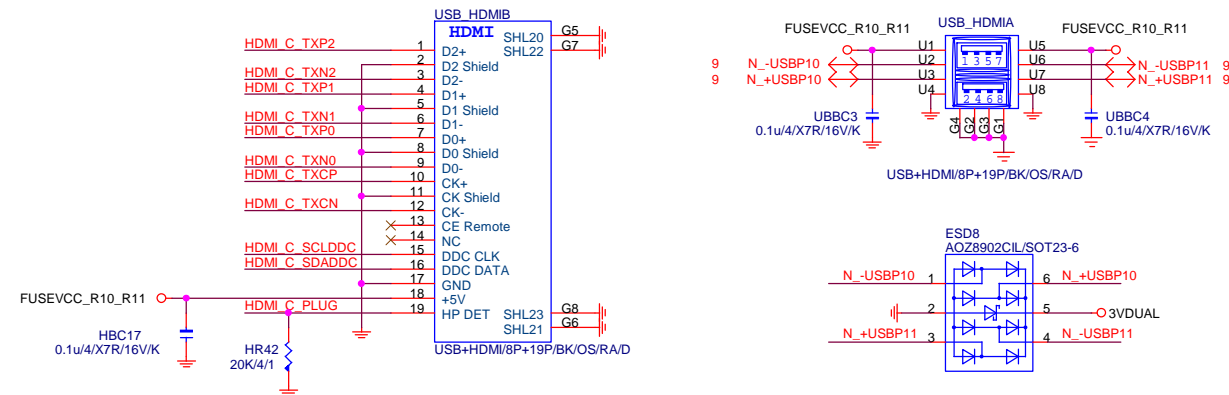
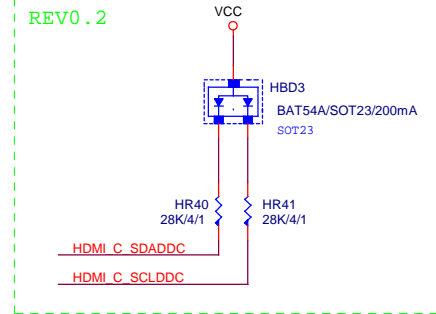
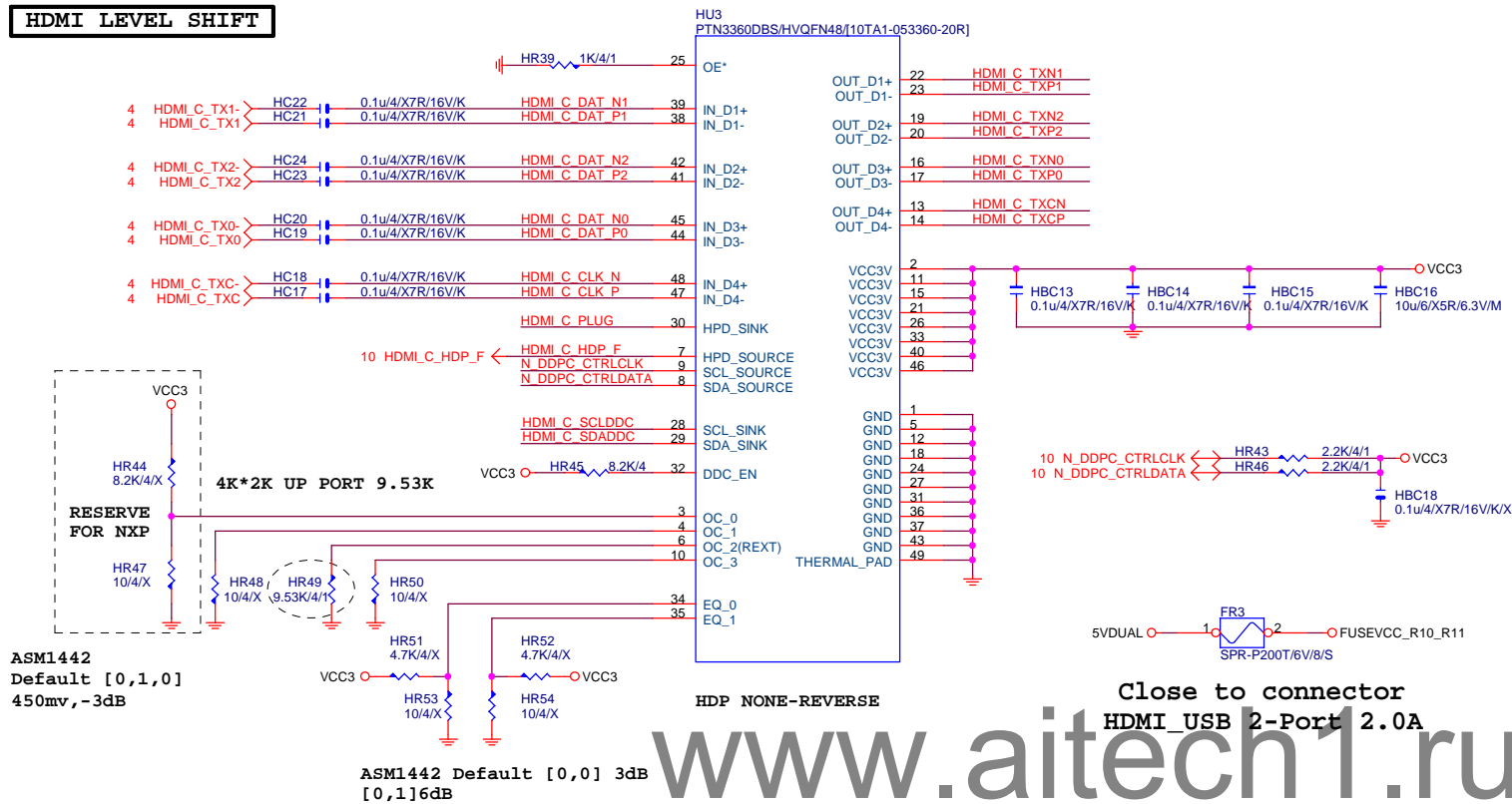
DVI LEVEL SHIFT



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Gigabyte Technology			
Title			
DVI			
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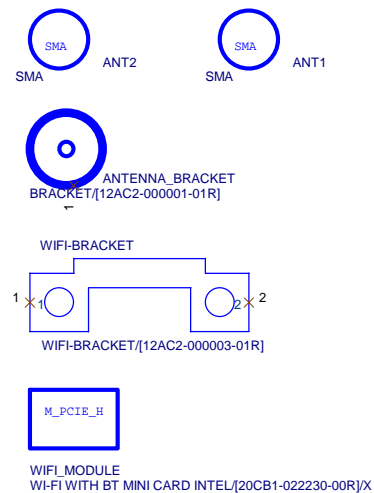
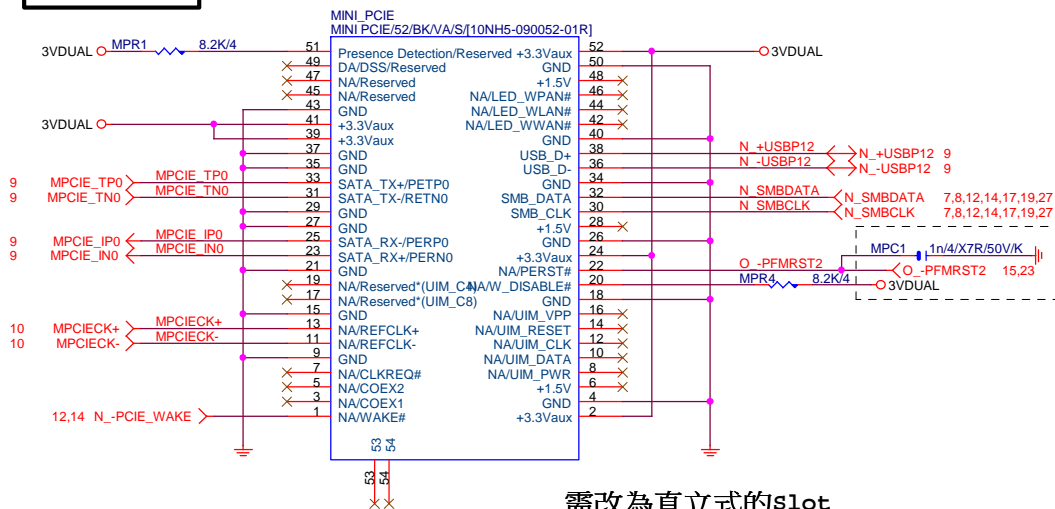
HDMI LEVEL SHIFT



Gigabyte Technology

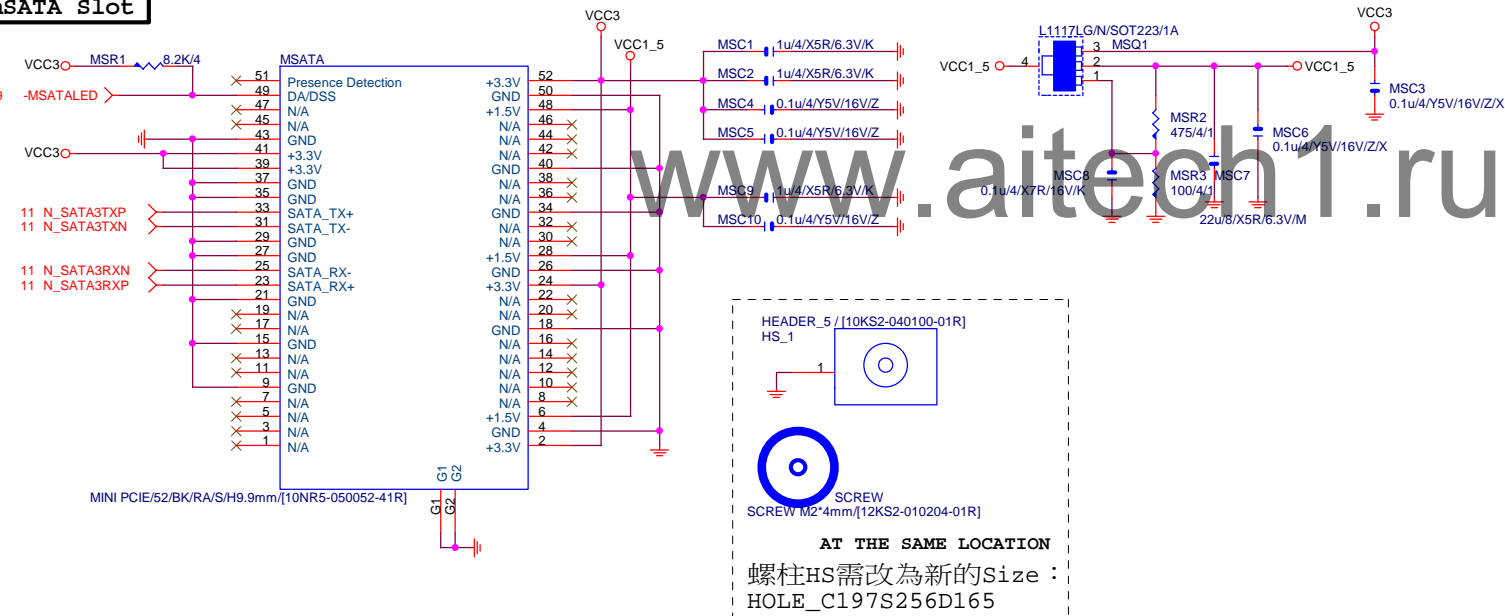
Title			HDMI + USB2.0 * 2	
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B				1.11
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Mini PCIe



需改為直立式的slot

mSATA Slot



AT THE SAME LOCATION
螺柱HS需改為新的Size
HOLE C197S256D165

Gigabyte Technology

Title	USB DAC POWER
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Size B	Document Number GA-B85N
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1.11

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